AMENDMENTS TO THE SPECIFICATION:

On page 1, kindly delete the present title and substitute the following:

~~MEMORY REDUNDANCY IMPLEMENTATION~~

MEMORY REDUNDANCE CIRCUIT TECHNIQUES

On page 1, line 6, after the heading "CROSS REFERENCE TO RELATED APPLICATION(S)," kindly insert the following new paragraph:

This is a continuation of Application No. 09/776,263 filed February 2, 2001.

Kindly amend the second paragraph on page 3, lines 7-28 as follows:

One type of basic storage element is the static random access memory (SRAM), which can retain its memory state without the need for refreshing as long as power is applied to the cell. In an SRAM device, the memory state II usually stored as a voltage differential within a bistable functional element, such as an inverter loop. A SRAM cell is more complex than a counterpart dynamic RAM (DRAM) cell, requiring a greater number of constituent elements, preferably transistors. Accordingly, SRAM devices commonly consume more power and dissipate more heat than a DRAM of comparable memory density[,]; thus efficient[;], lower-power SRAM device designs are particularly suitable for VLSI systems having need for high-density SRAM components, providing those memory components observe the often strict overall design constraints of the particular VLSI system. Furthermore, the SRAM subsystems of many VLSI systems frequently are integrated relative to particular design implementations, with specific adaptions of the SRAM subsystem limiting, or even precluding, the scalability of the SRAM subsystem design. As a result SRAM memory subsystem designs, even those considered to be "scalable", often fail to meet design limitations once these memory

subsystem designs are scaled-up for use in a VLSI system with need for a greater memory cell population and/or density.

On page 4, lines 2-33, kindly delete the present Summary of the Invention and substitute the following new Summary of the Invention:

The present invention is useful in a memory redundancy circuit in a memory module having a designated group of memory cells assigned to represent a logical portion of the memory structure and a redundant group of memory cells. In such an environment, according to a first exemplary method, the redundant group is assigned to the logical portion of the memory structure responsive to a preselected designated group condition.

The present invention also is useful in a memory circuit including pairs of designated memory cells and pairs of redundant memory cells. In such an environment, according to a second exemplary method, a signal path is redirected from the designated memory cells to the redundant memory cells based on a failure of the designated memory cells.

The present invention also is useful in a memory circuit including designated memory cells, redundant memory cells and a controller. In such an environment, according to a third exemplary method, a signal path is redirected from the designated memory cells to the redundant memory cells based on a failure of the designated memory cells. The controller may comprise a plurality of selectable switches having a logarithmic relationship to the number of designated memory cells.

Kindly amend the two consecutive paragraphs on page 36, line 23 through page 37, line 25 as follows:

FIG. 14 illustrates another aspect of the present invention which provides an implementation of row and column redundancy for a memory structure such as memory structure 100 in FIG. 1, or memory structure 300 in FIG. 3. This aspect of the present invention can be implemented by employing fuses that are programmable, for example, during production. Examples of such ~~uses~~fuses include metal fuses that are blown electrically, or by a focused laser; or a double-gated device, which can be permanently programmed. Although the technique can be applied to provide row redundancy, or column redundancy, or both, the present discussion will describe column redundancy in which both inputs and outputs may need the advantages of redundancy.

FIG. 14 shows an embodiment of this aspect of the invention herein having four pairs of columns 1402a-d with one redundant pair 1404. It is desirable to implement this aspect of the present invention as pairs of lines because a significant number of RAM failures occur in pairs, whether column or row. Nevertheless, this aspect of the present invention also contemplates single line redundancy. In general, the number of fuses in fuse box 1403 used to provide redundancy can be logarithmically related to the number line pairs, e.g., column pairs: $\log_2$ (number of column pairs), where the number of column pairs includes the redundant pairs as well. Because fuses tend to be large, their number should be minimized, thus the logarithmic relation is advantageous. Fuse outputs 1405 are fed into decoder circuits 1406a-d, e.g., one fuse output per column pair. A fuse output creates what is referred to herein as a "shift pointer". The shift pointer indicates the shift signal in the column pair to be made redundant, and subsequent column pairs can then be inactivated. It is desirable that the signals 1405 from fuse box [1410]1403 are decoded to generate shift signal 1412a-d at each column

pair. When shift signal 1412a-d for a particular column pair 1402a-d location is selected, as decoded from fuse signals 1405, shift pointer 1412a-d is said to be pointing at this location. The shift signals for this column, and all subsequent columns to the right of the column of pair shift pointer also become inactive.